What is claimed is:

1. An easy access dual ports structure, wherein said structure has a first port and a second port, and a CPU uses said dual ports structure to access said first port or said second port, said easy access dual ports structure comprising:

a first register bank for storing values of said first port, wherein said values comprise a first status value;

a second register bank for storing values of said second port, wherein said values comprise a second status value;

a global register for storing a control value and a mapped said first status value or mapped said second status value, or storing a control value, a mapped said first status value and mapped said second status value;

an address decoder coupling with said CPU to decode an address signal; and

a selector for selecting said first register bank or said second register bank to couple with said address decoder according to said control value stored in said global register, wherein said CPU can access said first register bank or said second register bank through said address decoder.

2. The easy access dual ports structure according to claim 1, wherein said values comprises a status value.

3. The easy access dual ports structure according to claim 1, wherein

said first register bank and said second register bank have a same address.

4. The easy access dual ports structure according to claim 1, wherein said second status value of said second register bank is mapped to said global register when said first register bank is coupled with said address decoder.

5. The easy access dual ports structure according to claim 1, wherein said first status value of said first register bank is mapped to said global register when said second register bank is coupled with said address decoder.

6. An easy access ports structure, wherein said structure has a plurality of ports, including a first to an N^{th} port, and a CPU uses said structure to access a port, said easy access ports structure comprising:

a plurality of register banks, including a first to an N^{th} register bank, for respectively storing values of said plurality of ports, wherein said values of each port comprise a status value;

a global register for storing a control value and mapped said at least (N-1) status values;

an address decoder coupling with said CPU to decode an address signal; and

a selector for selecting a corresponding register bank to couple with said address decoder according to said control value stored in said global register, wherein said CPU accesses said corresponding register bank through said address decoder.

7. The easy access dual ports structure according to claim 6, wherein said values of each port comprise a status value.

8. The easy access dual ports structure according to claim 6, wherein said plurality of register banks have a same address.

9. A method for accessing a dual ports structure, said dual ports structure comprising two register banks, a first and a second register bank, for respectively at least storing the status values of said two ports, a global register for at least storing a control value, and a CPU for using said dual ports structure to access one port of said two ports, wherein said method comprises:

coupling said first register bank to said CPU according to said control value for said CPU to access said first register bank; and

coupling said second register bank to said global register according to said control value for mapping said status value of said second register bank to said global register.

10. The method according to claim 9, wherein said mapping means to map the status value to said global register.

11. The method according to claim 9, wherein said first register bank and said second register bank have a same address.

12. A method for accessing a dual ports structure, said dual ports structure comprising two register banks, a first and a second register bank, for

respectively at least storing the status values of said two ports, a global register for at least storing a control value, and a CPU for using said dual ports structure to access one port of said two ports, wherein said method comprises:

coupling said first register bank to said CPU according to said control value for said CPU to access said first register bank; and

mapping said status values of said two register banks to said global register.

13. The method according to claim 12, wherein said mapping means to map the status value to said global register.

14. The method according to claim 12, wherein said first register bank and said second register bank have a same address.

15. A method for accessing a ports structure, said ports structure comprising a plurality of register banks, including a first to an N^{th} register bank, for respectively at least storing the status values of said a plurality of ports, a global register for at least storing a control value, and a CPU for using said ports structure to access one port of said a plurality of ports, wherein said method comprises:

coupling said first register bank to said CPU according to said control value for said CPU to access said first register bank; and

coupling said second to N^{th} register bank to said global register according to said control value for mapping said status values of said second to N^{th} register bank to said global register.

16. The method according to claim 15, wherein said mapping means to map the status value to said global register.

17. The method according to claim 15, wherein said first to N^{th} register bank have a same address.

18. A method for accessing a ports structure, said ports structure comprising a plurality of register banks, including a first to an N^{th} register bank, for respectively at least storing the status values of said a plurality of ports, a global register for at least storing a control value, and a CPU for using said ports structure to access one port of said a plurality of ports, wherein said method comprises:

coupling said first register bank to said CPU according to said control value for said CPU to access said first register ban; and

mapping said status values of said first to N^{th} register bank to said global register.

19. The method according to claim 18, wherein said mapping means to map the status value to said global register.

20. The method according to claim 18, wherein said first to N^{th} register bank have a same address.